



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:

30.08.2000 Bulletin 2000/35

(51) Int. Cl.⁷: **G11C 11/409**, **G11C 7/14**

(21) Application number: 00301259.8

(22) Date of filing: 17.02.2000

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 22.02.1999 US 253974

(71) Applicant:
STMicroelectronics, Inc.
Carrollton Texas 75006-5039 (US)

(72) Inventor: Guritz, Elmer Henry
Denton County, Texas 75022 (US)

(74) Representative:
Palmer, Roger et al
PAGE, WHITE & FARRER
54 Doughty Street
London WC1N 2LS (GB)

(54) **Reference voltage generator for an integrated circuit such as a dynamic random access memory (DRAM)**

(57) A reference voltage generator includes a voltage divider connected to a voltage supply and a feedback buffer amplifier. The divider supplies at least one voltage output signal to the feedback buffer amplifier under control of a feedback control signal supplied by the feedback buffer amplifier. The reference voltage generator may include a delay element coupled between the voltage divider and the feedback buffer amplifier in-line with the feedback control signal and a

low impedance output buffer that receives the voltage output signal from the voltage divider and supplies the reference voltage at an output node. The reference voltage may be supplied to the reference plates of bit storage capacitors within the memory cells. The storage capacitors can be protected by including a clamping circuit that maintains the output node at a voltage between the voltages of the two voltage supply terminals.

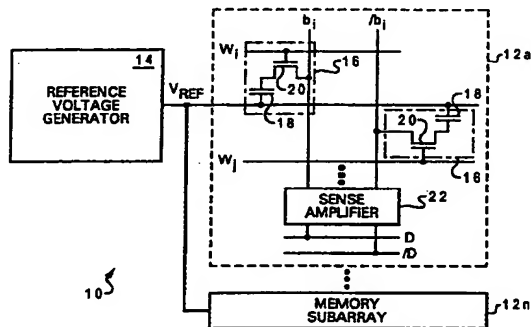


Fig. 1

Description

[0001] The present invention relates in general to integrated circuits and in particular to a reference voltage supply for an integrated circuit. Still more particularly, the present invention relates to a low impedance, low power reference voltage supply for an integrated circuit, such as a dynamic random access memory (DRAM), having high immunity to noise coupling.

[0002] A conventional dynamic random access memory (DRAM) includes an array of memory cells in which each memory cell includes a pass transistor and a capacitor. The capacitor functions as a memory element, with the presence of a charge on the capacitor representing a binary one and the absence of a charge representing a binary zero, for example. Data bits are read from and written to individual memory cells via word (row) and bit (column) lines connected to the pass transistors.

[0003] In a typical DRAM implementation, the reference plates of the memory cell capacitors are precharged to a voltage intermediate the supply voltage and ground. For example, U.S. Patent No. 5,255,232 to Foss *et al.* discloses that the reference plates of storage capacitors are precharged to half of the supply voltage in order to reduce voltage stress on the thin capacitor dielectrics. When precharging the reference plates of the capacitors, it is important that the plate reference voltage be immune to noise coupling so that noise does not couple through the storage capacitors and turn on the associated pass transistors, resulting in the loss of the data bits stored by the capacitors.

[0004] The present invention improves the immunity of a low impedance, low power reference voltage generator to noise coupling through the use of feedback control. In accordance with the present invention, a reference voltage generator, which may be utilized in an integrated circuit such as a dynamic random access memory (DRAM), includes a voltage divider connected to a voltage supply and a feedback buffer amplifier. The voltage divider, which determines the reference voltage, supplies at least one voltage output signal to the feedback buffer amplifier under control of a feedback control signal supplied by the feedback buffer amplifier. In at least one embodiment, the reference voltage generator further includes a delay element coupled between the voltage divider and the feedback buffer amplifier in-line with the feedback control signal and a low impedance output buffer that receives the voltage output signal from the voltage divider and supplies the reference voltage at an output node. When the reference voltage generator is implemented within a dynamic random access memory, the reference voltage is supplied to the reference plates of bit storage capacitors within the memory cells. The dielectrics of the bit storage capacitors can be further protected by including a clamping circuit within the reference voltage generator that maintains the output node at a voltage between the voltages of the two

voltage supply terminals.

[0005] All objects, features, and advantages of the present invention will become apparent in the following detailed written description.

[0006] The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1 is a high level block diagram of a dynamic random access memory (DRAM) with which a reference voltage generator in accordance with the present invention may advantageously be utilized;

Figure 2A depicts a voltage divider within an illustrative embodiment of a reference voltage generator in accordance with the present invention;

Figure 2B illustrates a feedback buffer amplifier within an illustrative embodiment of a reference voltage generator in accordance with the present invention;

Figure 2C depicts an output buffer within an illustrative embodiment of a reference voltage generator in accordance with the present invention; and

Figure 2D illustrates a clamping circuit within an illustrative embodiment of a reference voltage generator in accordance with the present invention.

[0007] With reference now to the figures and in particular with reference to Figure 1, there is illustrated a high level block diagram of a dynamic random access memory (DRAM) with which a reference voltage generator in accordance with the present invention may advantageously be utilized. DRAM 10 comprises a number of memory subarrays 12a-12n, which are each connected to a reference voltage generator 14 by a reference voltage signal V_{REF} . As shown, memory subarray 12a, which is illustrative of the construction of the remainder of memory subarrays 12, includes a number of memory cells 16 that each contain a capacitor 18 and a pass transistor 20. As is conventional, each capacitor 18 has a reference plate that is connected to reference voltage signal V_{REF} and a second plate that is connected to the source of the associated pass transistor 20. Each pass transistor 20 further includes a drain connected to a bit line (e.g., b_i), and a gate connected to a word line (e.g., w_i). Capacitors 18 function as memory elements, with the presence of a charge on a capacitor 18 representing a binary one and the absence of a charge representing a binary zero, for example. Data bits are read from and written to individual memory cells 16 by asserting an appropriate word line (w_i , w_j , etc.)

and by sensing or driving the appropriate complementary bit line pair (e.g., b_1 and \bar{b}_1). When performing a read access, data bits read out onto a complementary bit line pair are sensed and amplified to full rail voltage by a sense amplifier 22 and then output on complementary data bit buses D and \bar{D} .

[0008] As indicated in Figure 2A, Figures 2A-2D together form a circuit schematic of an illustrative embodiment of a reference voltage generator 14 in accordance with the present invention. The illustrative embodiment of reference voltage generator 14 includes the following five subcircuits: the voltage divider and a delay element shown in Figure 2A, the feedback buffer amplifier illustrated in Figure 2B, the output buffer depicted in Figure 2C, and the clamping circuit given in Figure 2D.

[0009] Referring first to Figure 2A, the voltage divider includes a number of transistors M4-M9, which in a typical integrated circuit embodiment are implemented as Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). As shown, transistors M4-M9, of which transistors M5, M8 and M9 are P-type and transistors M4, M6 and M7 are N-type, are connected in series between power supply voltage V_{DD} and ground. N-type transistor M7 has a gate input connected to a power-on (pwon) signal 30, and P-type transistor M9 has a gate input connected to the complemented power-on (pwonc) signal 32 generated by inverter I1. As a result, transistors M7 and M9 are switched off when memory arrays 12 are placed in sleep mode and switched on when memory arrays 12 are in active mode.

[0010] As shown, transistor M8 is connected to transistor M4 at node A, which is also connected to the gate input of transistor M4 and supplies N-drive (ndrv) output signal 36. Similarly, transistor M6 is connected to transistor M5 at node B, which is also connected to the gate input of transistor M5 and supplies P drive (pdrv) output signal 38. Transistors M4 and M5 are connected at node C, which is also connected to the substrate of transistor M5. The reference voltage V_{REF} which is determined by the relative sizes of transistors M6 and M8, is developed at node C when power-on (pwon) signal 30 is active. In a typical application, V_{REF} is half of V_{DD} ; however, by appropriate design of the sizes of transistors M6 and M8, V_{REF} may vary approximately 0.5 V from $V_{DD}/2$ for power supply voltages of 3.0 V to 3.6 V.

[0011] As further illustrated in Figure 2A, the gates of transistors M8 and M6 are both connected to a feedback (fdbk) control signal 34 received from the feedback buffer amplifier depicted in Figure 2B. Feedback control signal 34 is delayed by a delay element, such as transistor M12, in order to prevent instability in the feedback loop. Although a P-type transistor is preferred, alternative embodiments of the present invention may implement the delay element with an N-type transistor having its gate tied to V_{DD} or a resistor having an impedance of

150 k Ω or greater.

[0012] With reference now to Figure 2B, there is illustrated a feedback buffer amplifier within an illustrative embodiment of reference voltage generator 14. The feedback buffer amplifier includes an N-type transistor M0 and a P-type transistor M1 connected in series between V_{DD} and ground. The gates of transistor M0 and M1 are connected to N-drive and P-drive output signals 36 and 38, respectively. Transistors M0 and M1 are connected at node D, which is also connected to the substrate of transistor M1 and supplies feedback control signal 34 to the delay element. In order to ensure a quick response to the final steady state voltages of output signals 36 and 38 following power-on, transistors M0 and M1 have small sizes, and node D is lightly loaded.

[0013] The buffer amplifier shown in Figure 2B further includes an N-type transistor M10 connected to N-drive (ndrv) output signal 36 and a P-type transistor M11 connected to P-drive (pdrv) output signal 38. Transistors M10 and M11 turn off the gate drive voltages of transistors M0 and M1 when DRAM 10 is placed into sleep mode.

[0014] Referring now to Figure 2C, there is depicted a low impedance output buffer within an illustrative embodiment of a reference voltage generator 14. Reference voltage generator 14 includes one such output buffer for each respective memory subarray 12. As shown, the output buffer includes an N-type transistor M2 connected between V_{DD} and node E and a P-type transistor M3 connected in series with transistor M2 between node E and ground. As indicated, node E is further connected to the substrate of transistor M3 and may optionally be connected to a capacitor C1 to provide additional output stability. In order to achieve lower impedance and provide larger current capacity, transistors M2 and M3 are preferably large devices that are each sized with the same ratio with respect to an associated one of transistors M0 and M1. For example, if transistors M0 and M1 have length-to-width ratios of 8.0/0.8 μm and 12.0/0.8 μm , respectively, transistors M2 and M3 may be four times as large, having length-to-width ratios of 32.0/0.8 μm and 48.0/0.8 μm , respectively.

[0015] With reference now to Figure 2D, there is illustrated a clamping circuit within an illustrative embodiment of reference voltage generator 14 that serves to maintain each V_{REF} output of reference voltage generator 14 at a voltage between V_{DD} and ground (e.g., between 1.3 and 1.7 V) when DRAM 10 is in sleep mode. Thus, reference voltage generator 14 preferably includes one such clamping circuit for each respective memory subarray 12 of DRAM 10.

[0016] As depicted, the exemplary embodiment of a clamping circuit includes four N-type transistors (M14, M15, M17 and M19) and three P-type transistors (M13, M16, and M18) connected in series between V_{DD} and ground. Each of transistors M13-M19 is itself connected

is a diode configuration, that is, with its gate connected to its source, and each of P-type transistors M13, M16, and M18 also has a substrate connection to its drain. The voltage at which V_{REF} is maintained by the clamping circuit is determined by the sizes of transistors M13-M19, which in a preferred embodiment are all the same. By clamping V_{REF} at a voltage intermediate V_{DD} and ground when DRAM 10 is placed in sleep mode, the thin dielectric layer (e.g., SiO_2) of capacitors 18 within memory subarrays 12 are prevented from rupturing as a result of a voltage spike.

[0017] As been described, the present invention provides an improved reference voltage generator that may advantageously be utilized within an integrated circuit such as a DRAM. In the illustrative embodiment, the reference voltage generator includes several subcircuits, including a low-power voltage divider, a feedback delay element, a feedback buffer amplifier, a low impedance output buffer, and a protective clamping circuit. By introducing feedback control into the voltage divider, the present invention improves the immunity of the output reference voltage to noise in the power supply, while providing a quick response in response to power-on. The reference voltage generator has the further advantages of having a low-impedance output buffer that permits rapid charging of the reference plate of the memory array capacitors and a clamping circuit that protects the integrity of the capacitor dielectric during switching events.

[0018] While the invention has been particularly shown and described with reference to an illustrative embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

Claims

1. A reference voltage generator, comprising:

a voltage divider, connected to a voltage supply, that determines a reference voltage, wherein said voltage divider supplies at least one voltage output signal under control of a feedback control signal; and

a feedback buffer amplifier coupled to said voltage divider that receives said at least one voltage output and supplies said feedback control signal to said voltage divider.

2. A dynamic random access memory, comprising:

a reference voltage generator as recited in Claim 1; and

a memory array coupled to said reference voltage generator, wherein said memory array

includes a plurality of bit storage capacitors and at least one bit line for accessing said plurality of bit storage capacitors, and wherein each of said plurality of bit storage capacitors has a reference plate to which said reference voltage is supplied by said reference voltage generator.

3. A dynamic random access memory, comprising:

a reference voltage generator, including:

a voltage divider, connected to a voltage supply, that determines a reference voltage, wherein said voltage divider supplies at least one voltage output signal under control of a feedback control signal; a feedback buffer amplifier coupled to said voltage divider that receives said at least one voltage output and supplies said feedback control signal to said voltage divider; and

a memory array coupled to said reference voltage generator, wherein said memory array includes a plurality of bit storage capacitors and at least one bit line for accessing said plurality of bit storage capacitors, and wherein each of said plurality of bit storage capacitors includes a reference plate to which said reference voltage is supplied by said reference voltage generator.

4. The generator of claim 1 or the dynamic random access memory of claim 3, said voltage supply having first and second voltage supply terminals, wherein said voltage divider further comprises a plurality of transistors series connected between said first and second voltage supply terminals, each of said plurality of transistors having a respective control input, said feedback control signal being connected to control inputs of at least two of said plurality of transistors.

5. The generator or dynamic random access memory of Claim 4, said plurality of transistors including at least first, second, third, and fourth transistors, wherein said first transistor is coupled between said first voltage supply terminal and said second transistor and said fourth transistor is coupled between said second voltage supply terminal and said third transistor, and wherein said feedback control signal is connected to a control input of each of said first transistor and said fourth transistor.

6. The generator or dynamic random access memory of Claim 5, wherein said first transistor and said second transistor are coupled at a first node and

said third transistor and said fourth transistor are coupled at a second node, wherein said at least one voltage output signal includes a first voltage output signal connected to said first node and a second voltage output signal connected to said second node.

7. The generator of claim 1 or the dynamic random access memory of claim 3, and further comprising a delay element coupled between said voltage divider and said feedback buffer amplifier in-line with said feedback control signal.

8. The generator of claim 1 or the dynamic random access memory of claim 3, and further comprising an output buffer, coupled to said voltage divider, that receives said at least one voltage output signal and supplies said reference voltage at an output node.

9. The generator or the dynamic random access memory of Claim 8, wherein said output buffer has a low impedance relative to said feedback buffer amplifier.

10. The generator or the dynamic random access memory of Claim 8, said output buffer including a plurality of transistors connected in series, wherein said output node is a connection point of two of said plurality of transistors.

11. A dynamic random access memory, comprising:

a reference voltage generator, including:

a voltage divider, connected to a voltage supply, that determines a reference voltage, wherein said voltage divider supplies at least one voltage output signal under control of a feedback control signal;

a feedback buffer amplifier coupled to said voltage divider that receives said at least one voltage output and supplies said feedback control signal to said voltage divider;

a delay element coupled between said voltage divider and said feedback buffer amplifier in-line with said feedback control signal;

an output buffer, coupled to said voltage divider, that receives said at least one voltage output signal and supplies said reference voltage at an output node; and

a memory array including a plurality of bit storage capacitors and at least one bit line for

accessing said plurality of bit storage capacitors, wherein each of said plurality of bit storage capacitors has a reference plate coupled to said output node of said output buffer.

12. The generator or dynamic random access memory of Claims 8 or 11, said voltage supply including first voltage supply terminal and a second voltage supply terminal, said reference voltage generator further comprising:

a clamping circuit coupled to said output node and to said voltage supply, wherein said clamping circuit maintains said output node at a voltage between voltages of said first and second voltage supply terminals.

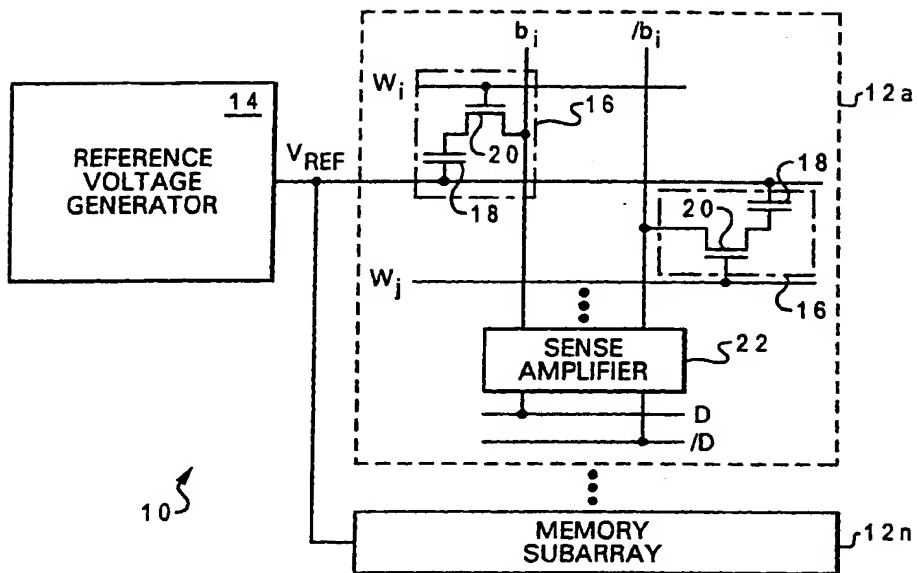


Fig. 1

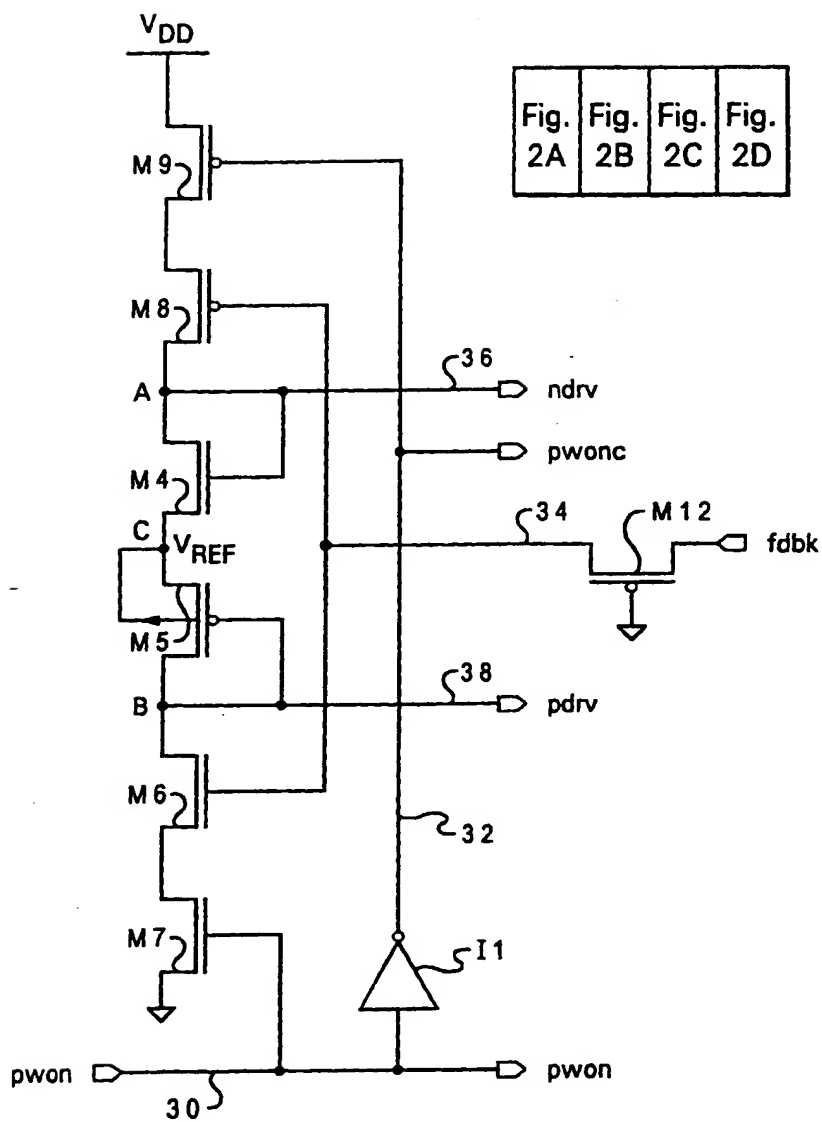


Fig. 2A

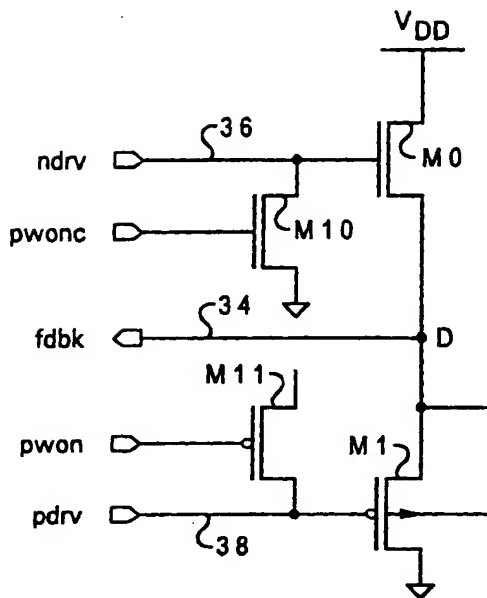


Fig. 2B

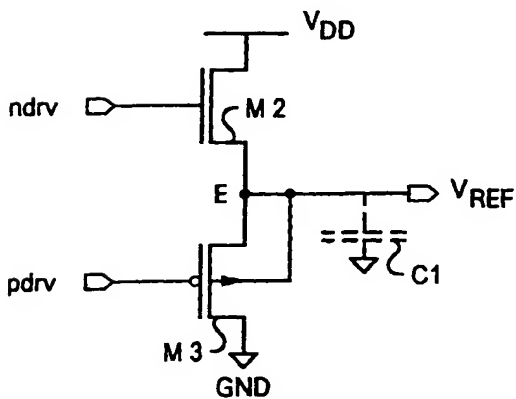


Fig. 2C

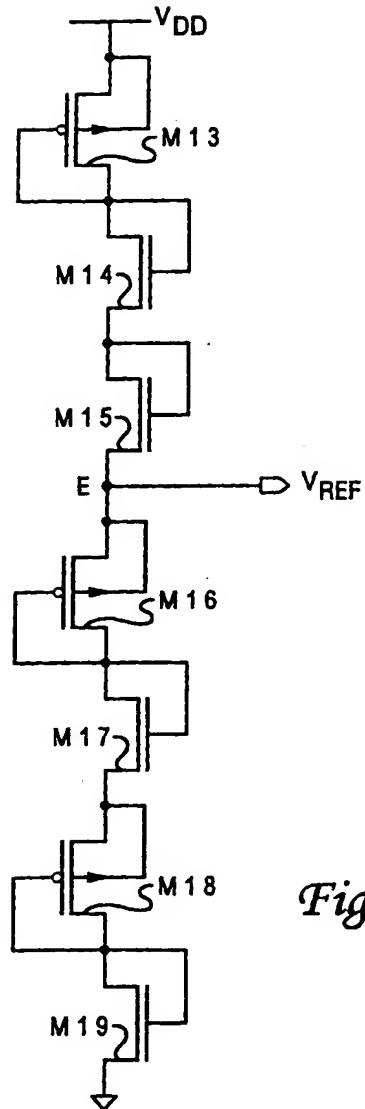
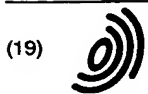


Fig. 2D



(19)

Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 1 031 990 A3

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
20.09.2000 Bulletin 2000/38

(43) Date of publication A2:
30.08.2000 Bulletin 2000/35

(21) Application number: 00301259.8

(22) Date of filing: 17.02.2000

(51) Int. Cl.⁷: G11C 11/409, G11C 7/14,
G11C 5/14, G05F 1/46,
G11C 11/407

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 22.02.1999 US 253974

(71) Applicant:
STMicroelectronics, Inc.
Carrollton Texas 75006-5039 (US)

(72) Inventor: Guritz, Elmer Henry
Denton County, Texas 75022 (US)

(74) Representative:
Palmer, Roger et al
PAGE, WHITE & FARRER
54 Doughty Street
London WC1N 2LS (GB)

(54) Reference voltage generator for an integrated circuit such as a dynamic random access memory (DRAM)

(57) A reference voltage generator includes a voltage divider connected to a voltage supply and a feedback buffer amplifier. The divider supplies at least one voltage output signal to the feedback buffer amplifier under control of a feedback control signal supplied by the feedback buffer amplifier. The reference voltage generator may include a delay element coupled between the voltage divider and the feedback buffer amplifier in-line with the feedback control signal and a low impedance output buffer that receives the voltage output signal from the voltage divider and supplies the reference voltage at an output node. The reference voltage may be supplied to the reference plates of bit storage capacitors within the memory cells. The storage capacitors can be protected by including a clamping circuit that maintains the output node at a voltage between the voltages of the two voltage supply terminals.

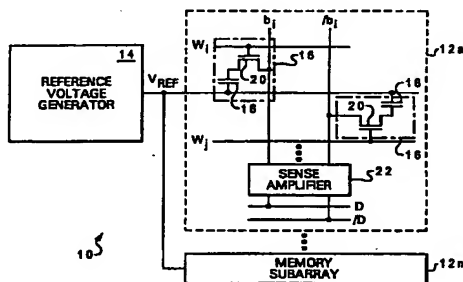


Fig. 1



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 30 1259

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 847 597 A (KOMIYA YUICHIRO ET AL) 8 December 1998 (1998-12-08) * figure 5 *	1,4-6, 8-10	G11C11/409 G11C7/14 G11C5/14 G05F1/46 G11C11/407
Y	---	12	
A	---	11	
X	US 5 212 440 A (WALLER WILLIAM K) 18 May 1993 (1993-05-18) * figure 4 *	1,4-6	
X	US 5 751 639 A (OHSAWA TAKASHI) 12 May 1998 (1998-05-12) * figure 7 *	1-3	
Y	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 09, 31 July 1998 (1998-07-31) & JP 10 092199 A (SAMSUNG ELECTRON CO LTD), 10 April 1998 (1998-04-10) * abstract *	12	
Y	US 4 438 346 A (CHUANG PATRICK T ET AL) 20 March 1984 (1984-03-20) * figures 1,5,7 * -----	12	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G11C G05F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 27 July 2000	Examiner Vidal Verdu, J.
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document</p>			

EPO FORM 1503 (03.02) (PUB.OFF)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 00 30 1259

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

27-07-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5847597 A	08-12-1998	JP 8171432 A KR 187804 B	02-07-1996 01-06-1999
US 5212440 A	18-05-1993	NONE	
US 5751639 A	12-05-1998	JP 8195081 A US 5854768 A US 5933383 A	30-07-1996 29-12-1998 03-08-1999
JP 10092199 A	10-04-1998	KR 200926 B DE 19724277 A GB 2316751 A,B US 5946242 A	15-06-1999 12-03-1998 04-03-1998 31-08-1999
US 4438346 A	20-03-1984	NONE	

EPO FORM P/418

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82